

Highly Efficient Switch-Mode 100-kV, 100-kW Power Supply for ESP Applications

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ABSTRACT

For nearly a century, electrostatic precipitators (ESP) were driven by line-frequency transformer-rectifier sets. The last decade has been marked by steady penetration of high-frequency HV power supplies (HVPS) that offer considerable benefits for the industry.

This paper describes a novel concept and physical demonstration of an ultra-high efficiency, small size and low cost HVPS specifically designed for ESP and similar markets. Key technology includes a modular HV converter with energy dosing inverters, which operate at above 50 kHz with and have demonstrated an efficiency of 97.5% in a wide range of operating conditions. The inverters' output voltages are phase-shifted, which yields an exceptionally low ripple of 1 % and a slew rate of 3 kV/ μ s combined with low stored energy. Modular construction allows easy tailoring of HVPS for specific needs. Owing to high efficiency, small size is achieved without turning to liquid cooling. Controls provide standard operating features and advanced digital processing capabilities, along with easiness of accommodating application-specific requirements.

HVPS design and testing are detailed. Experimental current and voltage waveforms indicate virtually lossless switching for widely-varying load in the full range of the line input voltages, and fair agreement with simulations. Calorimetric measurement of losses indicates to a >98.5% efficiency of the HV section. The overall efficiency is 95 % at full load and greater

than 90 % at 20-% load, with power factor typically greater than 93 %.

Keywords

Electrostatic Precipitator, ESP Power Supplies, High-Frequency Power Supplies, voltage multiplier

INTRODUCTION

For nearly a century, ESPs were driven by line-frequency transformer-rectifier sets. The last decade has been marked by a steady penetration of high-frequency HV power supplies (HVPS) that offer considerable benefits for the industry: small size, low ripple, fast response, etc., facilitating better collection efficiency. A good overview is provided by [1], [2]. It was noted that Alstom and NWL lead the market with hundreds of fielded units. Between other developments, work of Applied Plasma Physics [3], Genvolt [4], VEI [5] should be mentioned.

High conversion frequency, typically 20-25 kHz facilitates the size reduction. As noted in [2], the HV transformer of the Alstom SIR weighs about 225 lb, or 1/15 of that for a 60-Hz power supply. Other passive components are shrunk respectively.

Heat management is one of the main issues for reliability. It is done by air-cooling (NWL) or liquid cooling (Alstom). It should be noted that air-cooling schemes seem to be preferential in this industry. In order to realize high efficiency, almost universally, the converter part of the above HVPS makes use of series resonance to avoid switching losses. The theory and practice

This paper describes a novel concept and physical demonstration of an ultra-high efficiency, small size and low cost HVPS specifically designed for ESP and similar markets.

MAIN SPECIFICATIONS

1. Average output power 100 kW in the output voltage range of 90-100 kV; derated at lower voltage
2. High frequency ripple component: 1 % typically at 100 kV, full power.
3. Dynamic Response: slew rate 100 kV/ms min (5 % to 9.5% of preset voltage). Typically 300 kV/ms
4. Output Stored Energy: < 10 J.
5. Conversion frequency 50 kHz
6. Input Voltage: Three Phase 400 VAC +10 %, -14 %
7. Power Efficiency: typically > 95 % at full power at 100 kV, > 90 % at 20 kW.
8. Power factor: > 93% at full power at 100 kV, > 75% at 20 kW.
9. SPARK/ARC WITHSTAND
10. Overall weight 250 kg TBD; HV unit 109 kg (240 lbs); Oil volume less than 60 liter

KEY TECHNOLOGY

The HVPS is built around a modular HV converter (Figure 1). All converter modules M_1 - M_N are fed from a common Input Rectifier (IR). The modules comprise inverter INV_1 - INV_N feeding HV transformers T_1 - T_N that feed voltage multipliers R_1 - R_N , which voltages are summed by their DC outputs. Such topology may be termed as “inductive adder”. For the 100-kV, 100-kW rating $N=4$. Each module is built for 25-kV, 25-kW average power and must have high potential insulation of the secondary winding of the transformer rated at

3-25 kV=75 kVDC. This insulation must also withstand transient voltages arising during the HVPS turn-on and turn-off. The number of such transients is determined by the HVPS operating scenario, and mainly by the sparking rate.

The topology Figure 1 was investigated long ago [8], [9]. It allows reduction both of the number of the multiplier stages and the voltage rating of the HV transformer. The first improves the compression ratio and reduces drastically the stored energy. Phase shift of the inverters’ outputs voltages results in the decrease of the output ripple and in additional reduction of the stored energy. In this approach, the development costs and time are driven down noting that once a single module has been developed (including its main insulation), the whole system is realized by a simple combination of the desired number of modules. The penalty is larger part count and the necessity of high-potential insulation that is not required in conventional Cockcroft-Walton multipliers. However, this insulation is subjected mainly to DC stresses and therefore ages much slower compared to an AC stress.

The converter cells are centered around half-bridge energy dosing quasi-resonant inverters (Figure 2) [10], [11], [12]. The principle and theory of operation were put forward in [11]. In normal mode, one of the divider capacitors, C_{div} , is charged to the rail voltage. When the corresponding switch closes, it discharges through the primary, while its counterpart recharges to the rail voltage. If the current path contains an inductance, a sine waveform is generated, and ideally, all the energy stored in C_{div} would be transferred to the secondary side. If C_{div} discharges fully, and the current does not fall to zero, the free-wheeling diodes (FWD) across the capacitors clamp the current preventing the voltage reversal. Thus, the remainder of the energy stored in the circuit inductance is transferred to the output (see also Figure 4). The benefits of this topology are tight control of the energy transfer and inherent limitation of the short circuit current and voltages across the converter components.

The maximum frequency, at which the operation is possible with zero-current crossing (ZCC), in a normalized form, is given by the equation

$$f_N = \frac{1}{\frac{2}{\pi} \left[\frac{1}{2} a \cos\left(\frac{V_l}{V_l - E}\right) + \frac{E}{2V_l} \sqrt{1 - \frac{2V_l}{E}} \right]} \quad (*)$$

where E is the rail voltage, and both the rail voltage and the load voltage V_l are referenced to the same side of the transformer. The conversion frequency f is normalized to the resonant frequency f_0 of the loop formed by the leakage inductance and resonant capacitors: $f_N = f/f_0$.

A sample plot of this equation is shown in Figure 3. It should be noted that the real conversion frequency is somewhat lower to allow a deadtime of $\sim 1.5 \mu\text{s}$.

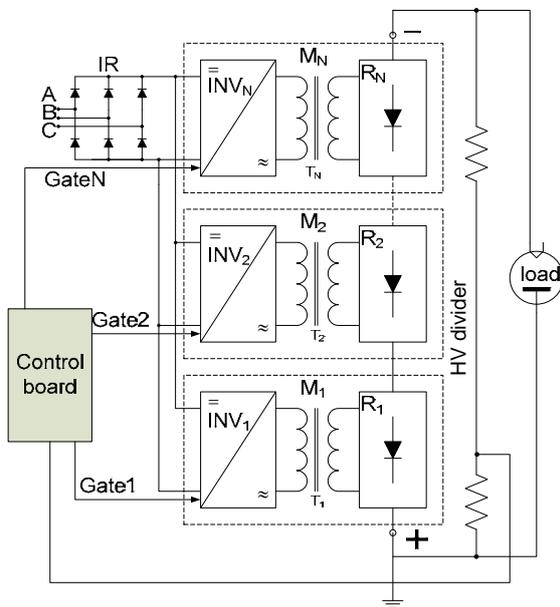


Figure 1. HVPS block-diagram.

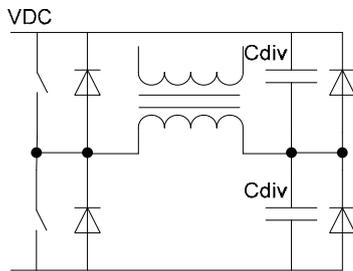


Figure 2. Inverter with energy dosing capacitors

The inverters operate at approximately 50 kHz at full load with virtually zero switching losses. The leakage inductance of the HV transformers is fully incorporated into the resonant tank circuits, so no external inductors are necessary.

Besides lowering the part count and cost, this feature is highly beneficial for the chosen multicell resonant topology, since leakage inductance is well repeatable from sample to sample and does not depend on temperature. Controls provide standard operating features and advanced digital processing capabilities, along with the easiness of accommodating application-specific requirements. The output regulation is accomplished by the frequency control.

EXPERIMENTAL

Single module

Typical waveforms shown in Figure 4 (taken at nominal line) indicate good resonant switching with no shoot-through currents in the full range of the line input voltages, and fair agreement with PSpice simulations. The primary winding was divided into two sections connected in parallel, each commutated by a transistor set, hence the notation “halved” in the figure caption. The dashed line shows the start of the FWD conduction. At low line, the FWDs do not conduct, and the converter operates in a boundary mode given by (*). These measurements were conducted with the Powerex IGBTs CM300DC-24NFM. The power losses were assessed at 50 W per transistor (four transistors, or 800 W per converter module), and the heat was easily evacuated using air-cooled heatsinks with overheat above ambient of less than 40°C . The methods of power loss measurement are detailed in [13].

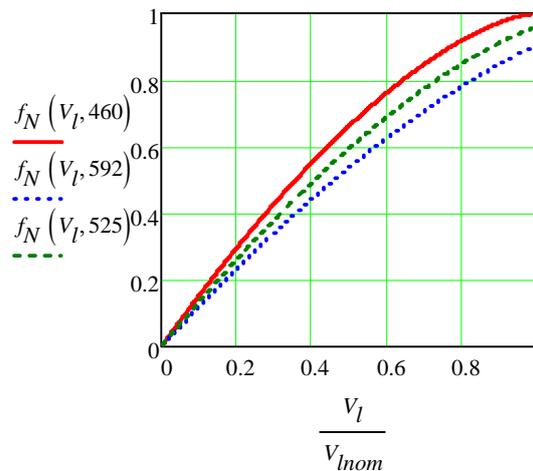


Figure 3. ZCC curves for low (460 V), high (592 V) and nominal (525 V) DC rail voltages. $V_{l, nom}$ is nominal load voltage.

Special attention was paid to the determination of the HV transformer and multiplier losses. This was key to the design of the HV tank. With this purpose, calorimetric measurements of the losses were performed. They yielded a figure of 344 W, with 175 W attributed to the transformer losses, and the rest to the multiplier losses. Thus, the efficiency of the HV section was expected to be >98.5%. Accounting also for the inverter losses, the converter efficiency was estimated at 97.5%, so the overall efficiency of 95% of the whole HVPS was projected. In view of the expected high efficiency, it was decided to adopt an air-cooling scheme.

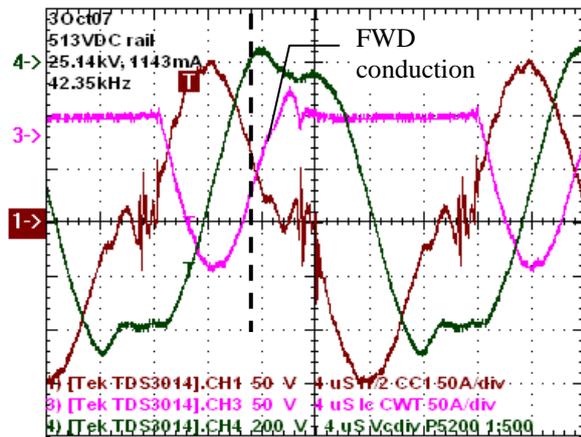


Figure 4. Nominal line. P=28.7kW. trace 1 – primary winding current (halved); trace 3 – collector current (halved); trace 4 – voltage across resonant capacitors. FWD conducts to the right of dotted line.



Figure 5. Laboratory HVPS.

HVPS Tests

A laboratory HVPS was assembled on a cart as shown in Figure 5. It comprises three main units: a circuit-breaker-protected line rectifier, an inverter section and an oil-filled HV tank. We note that in this work, the emphasis was on the converter part; the line rectifier was not optimized.

The HVPS was extensively tested with resistive loads. Figure 6, Figure 7 show typical phase-shifted primary windings currents (halved) for 100-kW and 50-kW operation, respectively. The oscillations after the main current surge are generated by the resonance between the leakage inductance and parasitic capacitance of the transformers. Note the absence of the “backswing” current pulse characteristic for the series resonant schemes under light load.

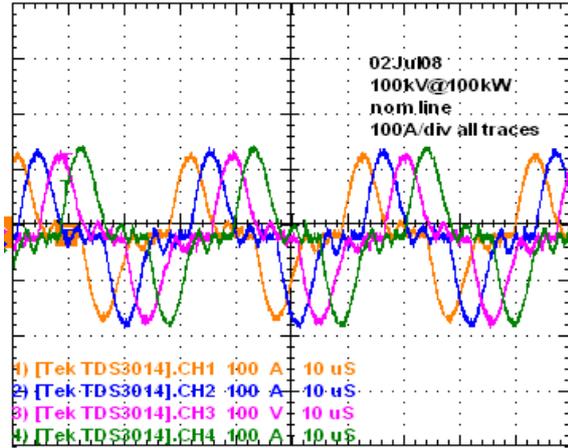


Figure 6. $\pi/4$ -phase-shifted primary windings currents (halved) at 100 kV@100 kW. Nominal line voltage 400 VAC.

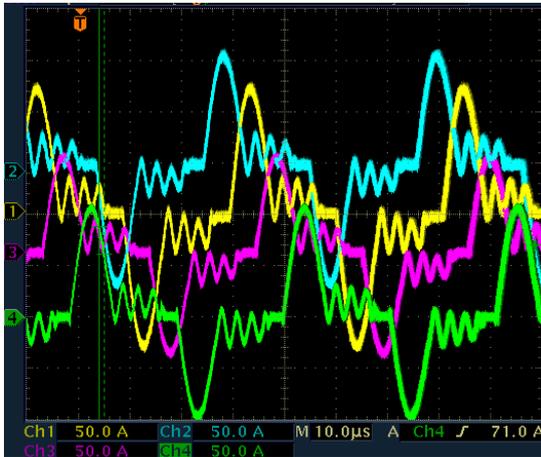


Figure 7. Same as in Figure 6 at 100 kV@50 kW. Low line 400 VAC-14 % (345 VAC).

Since the full-wave rectification scheme is used, the phase shift is $\pi/4$. PSpice calculations predict 0.223 % output voltage ripple peak-to-peak (p-p) with the HVPS shock capacitance of <2 nF (Figure 8) at the worst case of high line; the measured ripple is roughly four times larger, and has a lower frequency fundamental component (Figure 9), which can be attributed to the asymmetry of the gate signals, unequal parasitic capacitances, spread in winding data, etc. Similar effect was observed in [9]. These simulations provide also a value of the Power Factor (PF) of 0.943, which is close to the experimental results.

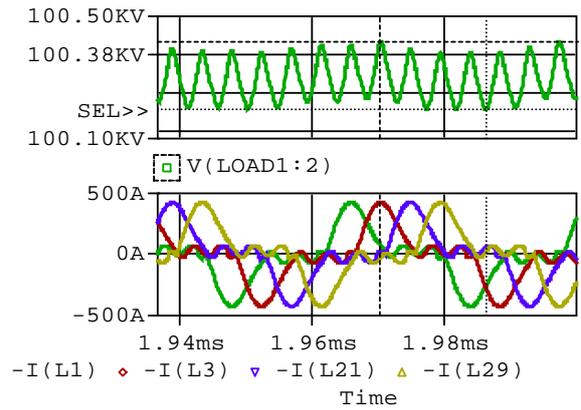


Figure 8. HVPS circuit simulation. High line 580 V. ripple 0.223 % p-p. PF=0.943. Experimental PF=0.946 (see Figure 11).

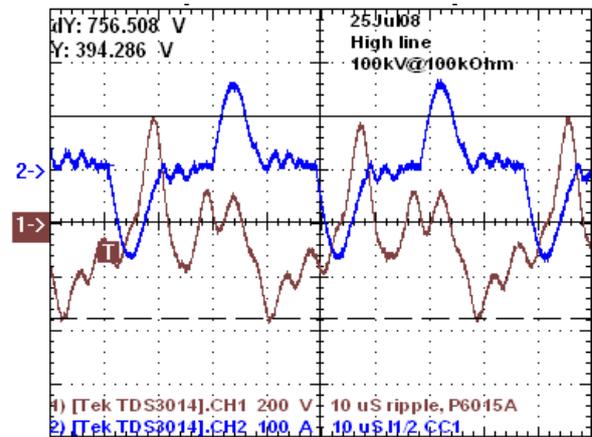


Figure 9. Ripple at 100 kV across 100-k Ω load is 0.762 % p-p.

The dynamic response of the HVPS is exceptionally fast: the risetime from zero to full output voltage is typically less than 250 μ s (Figure 10), depending on the line voltage. With fair accuracy, the dynamic characteristics can be analyzed using the equation

$$V_L(t) := 2 \cdot V_{rail} \cdot \sqrt{\frac{C_{div}}{C_s} \cdot f \cdot t}$$

where all the variables and parameters are reflected to the same side of the transformer; C_s is the overall capacitance of the module multiplier. If the frequency is varied during the charge, PSpice simulations provide much better accuracy.

Fast response is beneficial not only for ESP but medical applications as well. We note that the risetime practically does not depend on the load, since the load current is by an order of magnitude smaller than the current charging the multiplier capacitors.

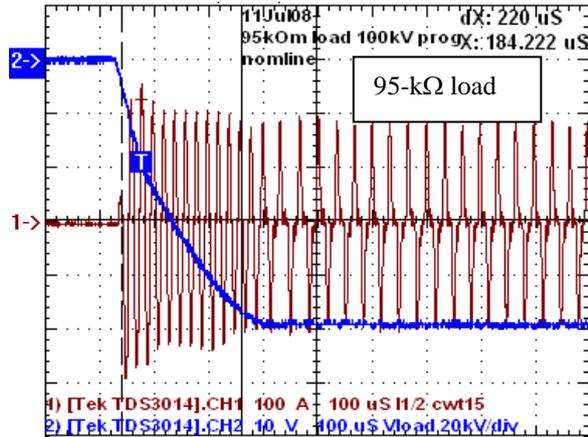


Figure 10. Risetime across 95-kΩ load at nominal line. Trace 2 – load voltage, 20 kV/div; trace 1 – primary current (halved), 100 A/div.

Figure 11 presents experimental data on the power measurements obtained at nominal line. In accordance with the simulations and information derived from the work with single module, the overall efficiency is 95 % at full load and greater than 90 % at 20-% load. The power factor was also satisfactorily high (compare to the simulation Figure 8). At high and low line, the measurements yielded very similar results. At higher resistance load, the efficiency and PF also stayed high (Figure 12).

At the time of writing this paper, long-term runs at 100 kV have been performed up to a power level of 75 kW. Full-power tests were limited to ~40 min. They showed conservative overheat of the major HVPS components. For the nominal line, the results are summarized in Table 1.

Table 1. Overheat of major HVPS components, °C.

load power, kW	transistor baseplate	FWD baseplate	HV tank
75	20	18	27
100	25	23	N/A

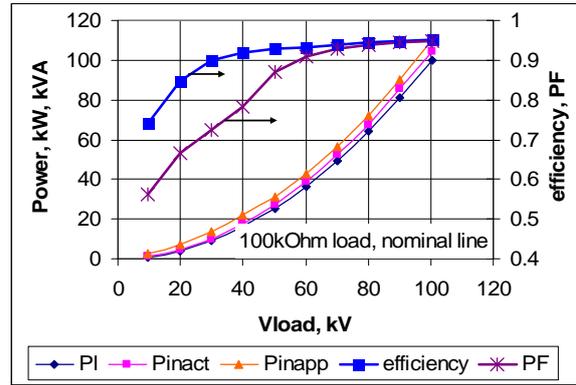


Figure 11. Apparent, P_{inapp} , and active input power, P_{inact} , load power, P_l , efficiency and PF at nominal line for 100-kΩ load.

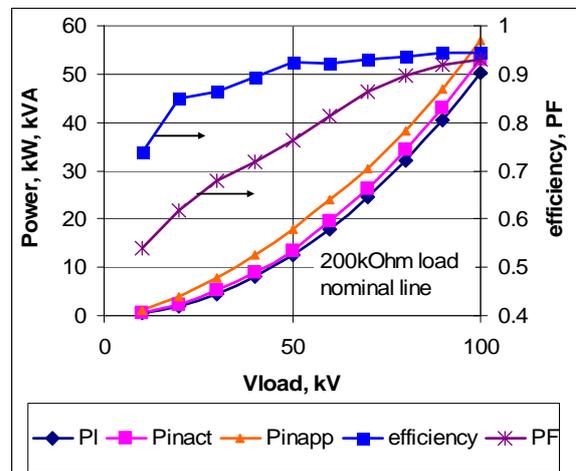


Figure 12. Same as in Figure 11 for 200-kΩ load.

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