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# A High-Power High-Voltage Power Supply for Long-Pulse Applications

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***Abstract*—This paper describes a concept and a physical demonstration of a high-efficiency small-size low-cost 100-kV 100-kW high-voltage (HV) power supply (HVPS) designed for long-pulse applications (units of milliseconds to dc operation). Key technology includes a modular HV converter with energy-dosing inverters that run at about 50 kHz and have demonstrated an efficiency of 97.5% across a wide range of operating conditions. The inverters' output voltages are phase shifted, which yields a low ripple of 1% and a slew rate of 3 kV/$\mu$s combined with less than 10 J of stored energy at the maximum voltage. Modular construction allows easy tailoring of HVPS for specific needs. Owing to high efficiency, small size is achieved without water cooling. Controls provide standard operating features and advanced digital processing capabilities, along with easiness of accommodating application-specific requirements. HVPS design and testing are detailed. It is shown that the ripple factor is inversely proportional to the number of modules squared. Experimental current and voltage waveforms indicate virtually lossless switching for widely varying load in the full range of the line input voltages and fair agreement with circuit simulations. The overall efficiency is as high as 95% at full load and greater than 90% at 20% load, with a power factor that is typically greater than 93%.**

***Index Terms*—Power electronics, pulsed power, resonant converter, voltage multiplier, voltage ripple.**

## I. Introduction

PULSED-POWER science and technology have accumulated many means of pulse generation in a wide range of parameters, with duration from picoseconds to seconds at power levels going up to terawatts for shorter pulses. A recent book by Mesyats [1] can serve as an encyclopedia on this subject. With the focus on *rectangular* millisecond-to-second durations, ubiquitous in X-ray tomography, RF sources, ion implantation, etc., the most common methods are using pulse-forming networks (PFN) or dc power supplies, self-modulated or having high-voltage (HV) switches for modulating the output voltage level. Obviously, PFNs are better suited for the generation of shorter pulses, and dc modulation is the only practical means of forming longer multimillisecond-to-several-seconds duration pulses with fast transitions. We include a single storage capacitor with a fully controlled output switch and inductive energy storage systems [2], [3] in the PFN category.

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The ability to provide fast rise time is beneficial also in electrostatic precipitation (ESP) applications. Heavy sparking inherent to the ESP operation results in frequent voltage collapses, and fast power restoration improves the collection efficiency [4], [5]. The same is true in the case of intermittent energization.

A typical requirement for dc HV power supplies (HVPSs), including but not limited to long-pulse applications, is the reduction of the output stored energy below a certain level, simultaneously meeting a contradicting requirement of keeping the voltage ripple as low as possible. The most promising approach to satisfy these conditions economically is using high-frequency (HF) multiphase topologies in their various incarnations. Closed-loop feedback circuits, in principle, can provide tight regulation and compensate for the line voltage variations, such as droop and line-frequency ripple, although it is not simple to ensure both clean and fast transitions without overshoots and high stability at a dc level. In order to realize high efficiency, almost universally, the converter part makes use of resonance to avoid switching losses. The theory and practice of such converters are known well [6], [7]. Very high power systems have been developed around three-phase HV transformers having individual or common cores [8]–[10] that operate typically at 20 kHz. A natural way for the voltage/current adjustment in such converters is frequency regulation.

We favor a modular approach that makes use of multiple phase-shifted individual transformers, each having its rectifying circuit [11], [12]. In this way, the system design is flexible and open, with the possibility of choosing the desired number of phases for the ripple suppression. This paper widens this concept and describes a physical demonstration of an ultrahigh-efficiency small-size low-cost 100-kV 100-kW HVPS designed for long-pulse applications. It is also suitable for ESP and similar markets.

## II. Short Specifications

This section is intended as a short introduction to the following material, giving a brief outline of the specifications that guided the development and have been largely met or exceeded. The emphasis is on the dynamic characteristics combined with high power. The main specifications are as follows:

1) average output power: 100 kW in an output voltage range of 90–100 kV; derated at lower voltage;
2) dynamic response: a slew rate of 100 kV/ms minimum (5% to 95% of preset voltage); typically 300 kV/ms;

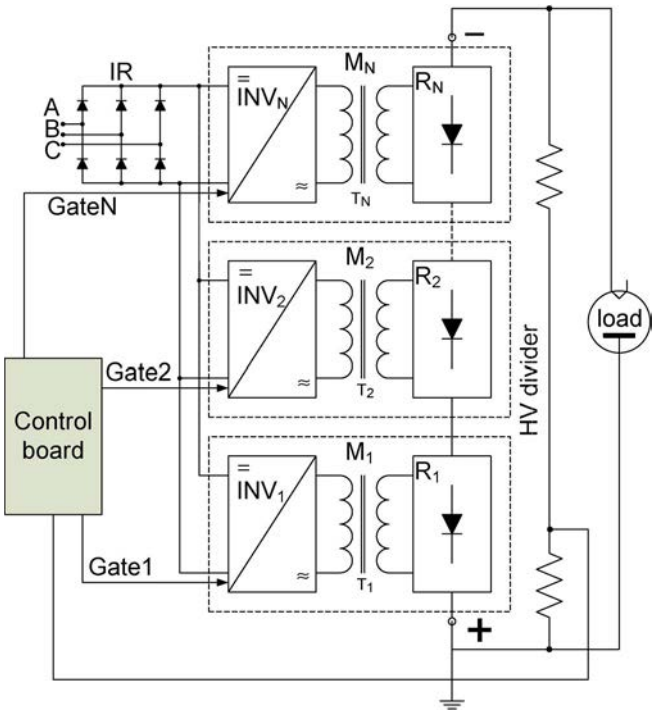


Fig. 1. HVPS block diagram.

3) HF ripple component, peak to peak (p-p): 1% typically at 100 kV at full power;
4) output stored energy: $< 10$ J;
5) conversion frequency: 50 kHz;
6) input voltage: three-phase 400 VAC$^{+10\%}_{-14\%}$;
7) power efficiency: typically $> 95\%$ at full power at 100 kV; $> 90\%$ at 20 kW;
8) overall weight: $< 250$ kg; oil volume less than 60 L.

## III. Key Technology

The HVPS is built around a modular HV converter (Fig. 1). All converter modules $M_1 - M_N$ are fed from a common input rectifier (IR). The modules comprise inverters $INV1 - INVN$ feeding HV transformers $T_1 - T_N$ that feed voltage multipliers $R_1 - R_N$ having $M$ multiplication stages, which voltages are summed by their dc outputs. Such topology may be termed as "inductive adder." For the 100-kV 100-kW rating, $N = 4$, and $M = 3$. Each module is built for 25-kV 25-kW average power and has high-potential insulation of the secondary winding of the transformer rated at $3 \cdot 25$ kVDC $= 75$ kVDC. This insulation, along with the rest of the components (mainly HV capacitors), must also withstand transient voltages arising during the pulsing. The number of such transients is determined by the HVPS operating scenario. For instance, in ESP applications, the number of pulses during the lifetime is determined by the sparking rate. If the latter is 6 sparks/min, the number of shots may well exceed $10^7$.

The topology Fig. 1 was suggested and partially investigated long ago [11], [12]. It allows reduction of both the number of multiplier stages and the voltage rating of the HV transformer. The first improves the compression ratio (the ratio of the voltage across the first multiplier stage to that of the last) and reduces drastically the stored energy. With $M = 3$, the transformers and multiplier boards are rated at 8.5 kV, which simplifies their design and greatly reduces the insulation stress caused by the HF voltage component. The phase shift of the inverters' output voltages results in the decrease of the output ripple and in the additional reduction of the stored energy. In this approach, the development costs and time are driven down, noting that, once a single module has been developed (including its main insulation), the whole converter is realized by a simple combination of the desired number of modules that may be connected both in series and in parallel. The penalty is larger part count and the necessity of the high-potential main insulation that is not required in conventional Cockroft-Walton multipliers. However, this insulation is stressed mainly by a dc voltage and therefore ages much slower compared to an HF (tens of kilohertz) stress [13]. Under pulsed operation, the main insulation is also subjected to pulse voltages.

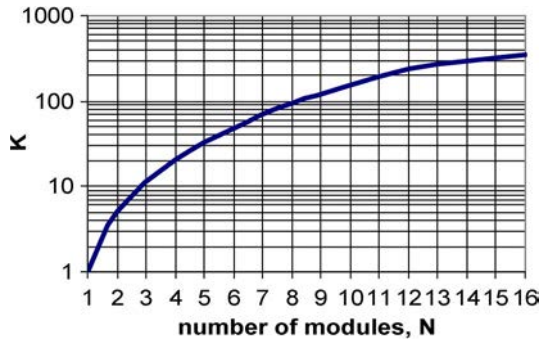


Fig. 2. Ripple suppression factor.

### A. Ripple Suppression

Let us define the ripple suppression factor $K$ as the ratio of the ripple of the HVPS comprising $N$ modules operating in-phase $V_{Nns}$ to that having $N$ phase-shifted modules $V_{Ns}$. The ripple can be regarded as the p-p voltage of the HF ac component or can be represented in percent of the dc component. For simplicity sake, we will assume here that the rectified voltage of each module is a superposition of a dc component and a modulus of a sine wave.

The ripple suppression factor can be easily calculated; it is shown in a graphical form in Fig. 2. It is shown that, for the analyzed case, $K$ is proportional to $N^2$. For arbitrary ripple waveforms, this dependence is more complicated. In general, $K$ can be estimated using the formula $K = \alpha \cdot N^{\beta}$, where the waveform-dependent coefficient $\alpha \approx 1 \div 1.3$ and the exponent $\beta = 1 \div 2$. For a rectified sine wave, $\alpha \approx 1.3$ and $\beta = 2$, as shown in Fig. 2, whereas for a sawtooth ripple defined, for instance, by a function $\nu(t) = -t + ceil(t)$, $\alpha = 1$ and $\beta = 1$ (this statement can be also easily verified graphically).

If the ripple factor is specified, the phase shift imparts approximately $N$ to $N^2$ reduction of the rise time, output capacitance, and the stored energy. Thus, the described multicell concept enables the HVPS optimization in the space of the aforementioned parameters.

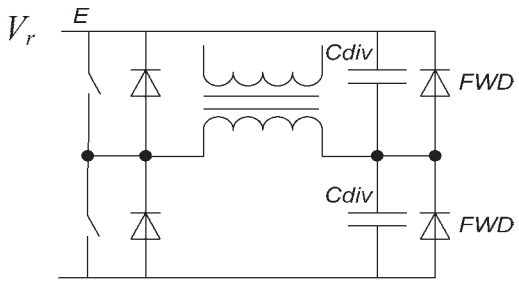


Fig. 3. Half-bridge inverter with energy-dosing capacitors. $V_r$ denotes the dc rail supply voltage.

### B. Individual Module Design

The converter cells are centered around half-bridge energy-dosing quasi-resonant inverters (Fig. 3). The principle, theory of operation, benefits, and shortcomings were described elsewhere [14] (see also the accompanying paper [15] and its references), and we do not expand the description here.

The inverters operate at approximately 50 kHz at full load with virtually zero switching losses. The leakage inductance of the HV transformers is fully incorporated into the resonant tank circuits; thus, no external inductors are necessary. Aside from lowering the part count and cost, this feature is highly beneficial for the chosen multicell resonant topology, since leakage inductance is well repeatable from sample to sample and, being determined by the flux concentrated outside the ferromagnetics, virtually does not depend on temperature. The parasitic capacitance of the transformer has larger technological tolerances. It is also more sensitive (than the leakage inductance) to the transformer-rectifier position. However, these factors can affect the voltage sharing between the modules only at a no-load scenario, and by a proper choice of the conversion frequency, this effect can be nullified [16].

### C. Control

The control board is based around FPGA. It provides standard operating features and advanced digital processing capabilities, along with the easiness of accommodating application-specific requirements. The standard features include multiple protections (arc/spark, overheat of the major components, overcurrent and overvoltage, etc.) and means of voltage and current setting. The output regulation is accomplished by the frequency control and is realized digitally, with the FPGA forming the transistors' conduction intervals to realize ZCS. In such a way, the switching losses are virtually eliminated, which allows using relatively slow inexpensive transistors having low saturation voltage; the latter also boosts the inverter efficiency.

The feedback loop taking the control signal from a precision high-bandwidth built-in HV divider is optimized for fast transitions with minimal or no overshoot (see experimental sections hereinafter) and tight stabilization after the voltage settling. We note here that full-scale HVPS PSpice models were developed. They adequately reproduce all salient features of the HVPS operation, including parasitic components of the HV part, the phase-shift mechanism, feedback circuit, etc., assisting in both the design and interpretation of the experimental data.

## IV. Experimental

### A. Measurement Means and Experimental Methods

For the HF current measurement, specialty workshop-made current transformers with a sensitivity of 0.01 V/A (designated further in the text as CC1) and Rogowski probes of PEM make, model CWT15 [17], were used. The latter were also used for the CC1 calibration. A standard high-precision Spellman voltage divider (model HVD100 [18]) served for the HVDC measurement. A modified, compensated, and calibrated version, designated as HVD100C, was used for the transient measurements. Its rise time is less than 2 $\mu$s. The ripple was monitored by a specialized ripple checker comprising a blocking capacitor in series with a resistor [19], the voltage across which was measured by a P6015A Tektronix probe. Although the ripple did not exceed 1 kV at dc operation, such HV probe was needed to accommodate much higher transient voltages during turn-on. Floating voltage measurements were performed by a differential Tektronix probe P5200. A specialized nonlinear divider (workshop made) was used for the measurement of saturation voltages across the semiconductor switches [20]. Power measurements [efficiency and power factor (PF)] were taken with a Voltech power meter, model PM300. Temperatures were monitored by thermocouples connected to an Agilent data logger, model 34970A, with supporting BenchLink software.

The input line voltage was regulated manually with a three-phase variac in tests with a single module, at a power level of less than 30 kW. Thus, the input voltage could be adjusted continuously. At higher power, a three-phase line-frequency transformer with switchable taps was used. It allowed the simulation of the scenarios of low-, nominal-, and high-line input voltages. The latter were not stabilized and varied slightly during the runs. The point of measurement was the dc rail supply voltage $V_r$. In this paper, the values of the latter corresponding to the aforementioned scenarios are defined as the ranges from 460 to 480 V, 510 to 530 V, and 580 to 600 V for the low-, nominal-, and high-line input voltages, respectively. The $V_r$ variation from 460 to 590 V corresponds to the three-phase 400 $\mathrm{VAC}^{+10\%}_{-14\%}$ line factoring in the voltage drop in the IR.

### B. Single Module Tests

Typical waveforms shown in Fig. 4 indicate good resonant switching with no shoot-through currents in the full range of the line input voltages, and fair agreement with PSpice simulations. In this and the following figures, the inset notes indicate test conditions, types of the probes used, horizontal and vertical resolutions, etc. The primary winding was divided into two sections connected in parallel, each commutated by a transistor set, hence the notation "halved" in this and the following figure captions. The dashed line shows the start of the FWD conduction. At low line, the FWDs do not conduct at all. These measurements were performed with the Powerex IGBTs CM300DC-24NFM. The power losses were assessed at 50 W per transistor, and the heat was easily evacuated using air-cooled heat sinks with an overheat of less than 40 °C above

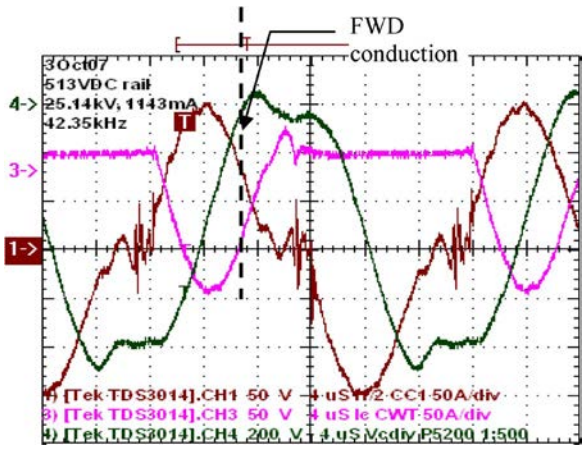


Fig. 4. Nominal line. $P = 28.7$ kW. (Trace 1) Primary winding current (halved). (Trace 3) Collector current (halved). (Trace 4) Voltage across resonant capacitors. FWD conducts to the right of the dotted line.

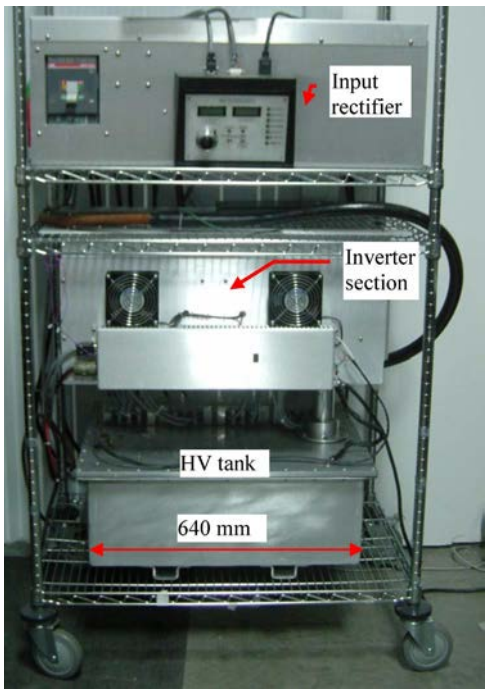


Fig. 5. Laboratory HVPS.

ambient under the harshest conditions. The methods of power-loss measurement and calculation are detailed in [20].

Special attention was paid to the determination of the HV transformer and multiplier losses. This was a key to the design of the HV tank. With this purpose, the calorimetric measurements of the losses of the converter module HV components were performed. The converter efficiency was estimated at 97.5%; thus, an overall efficiency of 95% of the whole HVPS was projected. In view of the expected high efficiency, it was decided to adopt an all-air-cooling scheme without any heat exchangers.

### C. HVPS Tests

A laboratory HVPS was assembled on a cart, as shown in Fig. 5. It comprises three main units: a circuit-breaker-protected line rectifier (the heaviest unit), an inverter section, and a hermetically sealed oil-filled HV tank. The latter weighs 109 kg and contains less than 60 L of oil. We note that, in this paper, the emphasis was on the converter part; the line rectifier was not optimized for size and cost.

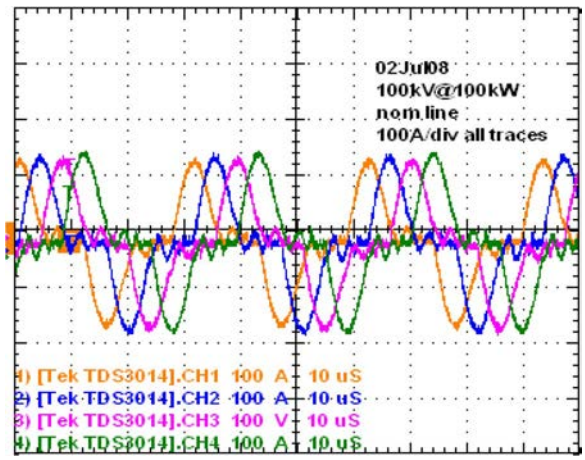


Fig. 6. $\pi/4$-phase-shifted primary winding currents (halved) at 100 kV and 100 kW. Nominal-line voltage: 400 VAC.

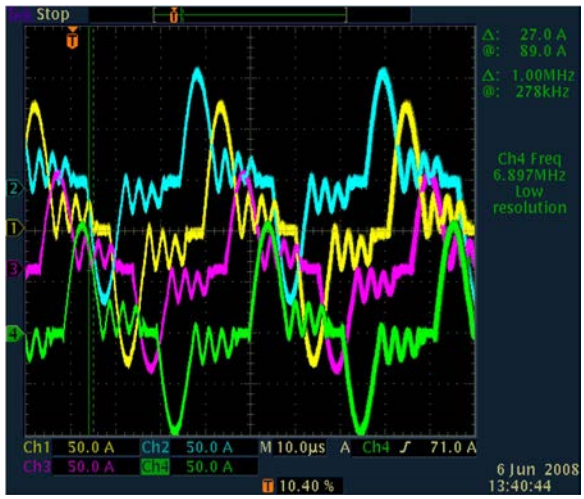


Fig. 7. Same as in Fig. 6 at 100 kV and 50 kW. Low-line voltage: 400 VAC-14% (345 VAC).

The HVPS was extensively tested with resistive loads. Figs. 6 and 7 show typical phase-shifted primary winding currents (halved) for 100- and 50-kW operations, respectively. The oscillations after the main current surge are generated by the resonance between the leakage inductance and parasitic capacitance of the transformers. Note the absence of the "backswing" current pulse; the latter characterizes true series resonant schemes under light load.

Since a full-wave rectification scheme is used, the phase shift between the transformer windings' currents is $\pi/4$. PSpice calculations predict 0.223% output voltage p-p ripple with an HVPS shock (output) capacitance of $< 2$ nF at the worst case of high line (Fig. 8). The measured ripple is roughly four times larger and has a lower frequency fundamental component (Fig. 9). The emergence of the latter can be attributed to the asymmetry of the gate signals, unequal parasitic capacitances,

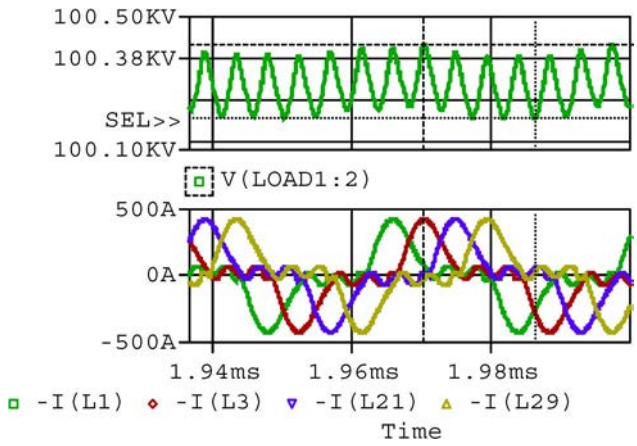


Fig. 8. HVPS circuit simulation. High-line voltage: $V_r = 580$ V. Ripple: 0.223% p-p. $PF = 0.943$. Experimental $PF = 0.946$ (see Fig. 11).

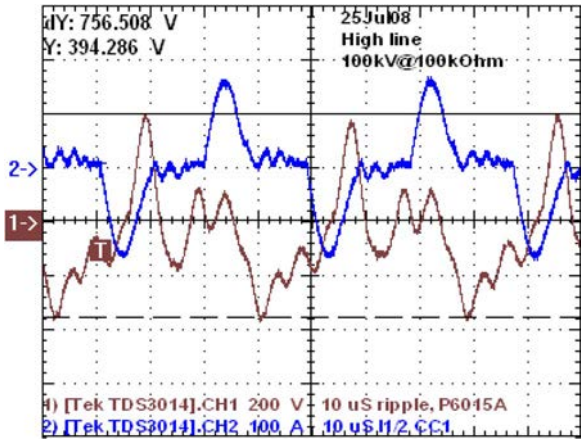


Fig. 9. Ripple at 100 kV across 100-kΩ load is 0.76% p-p. High line.

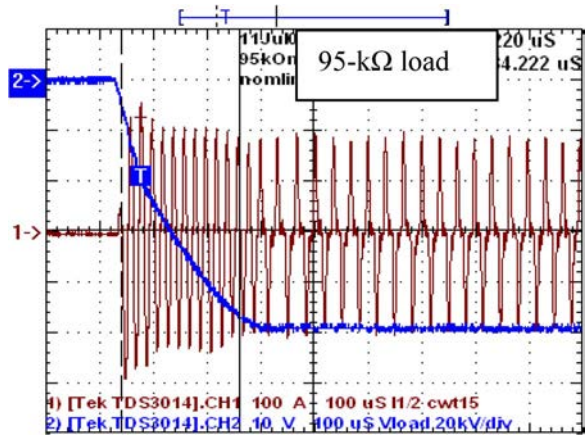


Fig. 10. Rise time across 95-kΩ load at nominal line. (Trace 2) Load voltage: 20 kV/div (measured by a specialty compensated voltage divider). (Trace 1) Primary current (halved): 100 A/div.

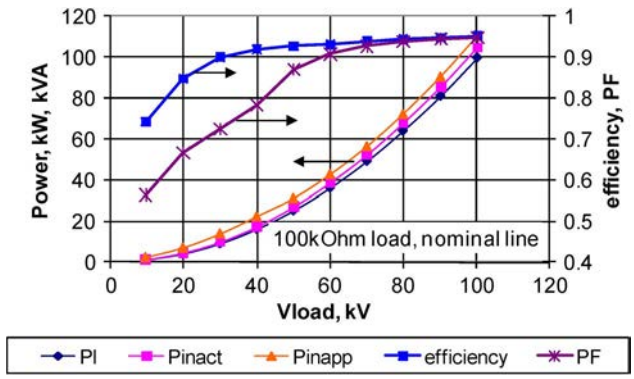


Fig. 11. Apparent (Pinapp) and active (Pinact) input powers, load power (Pl), efficiency, and PF at nominal line for 100-kΩ load.

spread in the winding data, nonideal feedback, etc. Similar effect was observed in [12]. The aforementioned simulations provide also a value of the PF of 0.943, which is close to the experimental results. Note that the ripple wave shapes are neither a rectified sine wave nor sawtooth; they are but closer to the first pattern; thus, the value for the exponent in (4) can be adopted as $\beta = 2$. This is borne out by numerous measurements and simulations in a wide range of the load impedances and output voltages. Again, poor feedback can strongly affect the ripple suppression by the phase shift.

Accounting for a very conservative voltage rating of the HV transformers and low ripple, the dynamic response of the HVPS is exceptionally fast: The rise time from zero to full output voltage is typically less than 250 $\mu$s (Fig. 10), depending on the line voltage. With fair accuracy, the dynamic characteristics in the energy-dosing mode can be analyzed using [14]

$$V_l(t) = 2V_r\sqrt{\frac{C_{\text{div}}}{C_s}ft} \tag{1}$$

where all the variables and parameters are reflected on the same side of the transformer; $t$ is the time, $f$ is the conversion frequency, and $C_s$ is the overall capacitance of the module multiplier and load. If the frequency is varied during the charge, PSpice simulations provide better accuracy. Obviously, the rise time, as derived from (1), the output stored energy, and the ripple factor are inversely proportional to $C_s$. Thus, allowing for a 2-% ripple factor at full voltage and full power, the rise time can be reduced to less than 100 $\mu$s. We note that the rise time practically does not depend on the load, since the load current is by an order of magnitude smaller than the current charging the multiplier capacitors.

Fig. 11 shows the experimental data on the power measurements obtained at the nominal line. In accordance with the simulations and information derived from the work with the single module, the overall efficiency is 95% at full load and is greater than 90% at 20% load. The PF was also satisfactorily high. At high and low lines, the measurements yielded very similar results. At higher resistance load, the efficiency and PF were virtually the same (Fig. 12).

The long-term runs at 100 kV have been performed up to a power level of 100 kW (average continuous power). In order to establish the overload capability, the HVPS was also run with three modules at 88.4 kV, 90 kW, and in a pulsed mode (see the following). Conservative overheat of the major HVPS components was observed. For the nominal line, the results are summarized in Table I.

The HVPS was also tested in a pulsed mode, mainly with the goal of validating the lifetime of the main insulation. The HVPS-generated 110-kV rectangular pulses with a period of

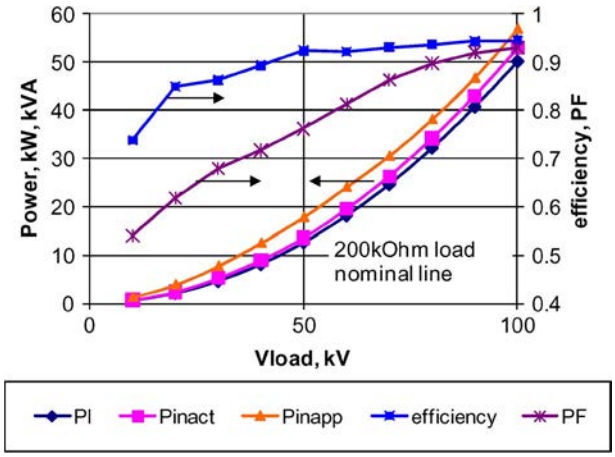


Fig. 12. Same as in Fig. 11 for 200-kΩ load.

TABLE I
OVERHEAT OF MAJOR HVPS COMPONENTS, °C

| load power, kW | transistor baseplate | FWD baseplate | HV tank (bulk oil) |
|---|---|---|---|
| 100 (4 modules) | 25 | 23 | 42 |
| 90 (3 modules) | 27 | 10 | 38 |

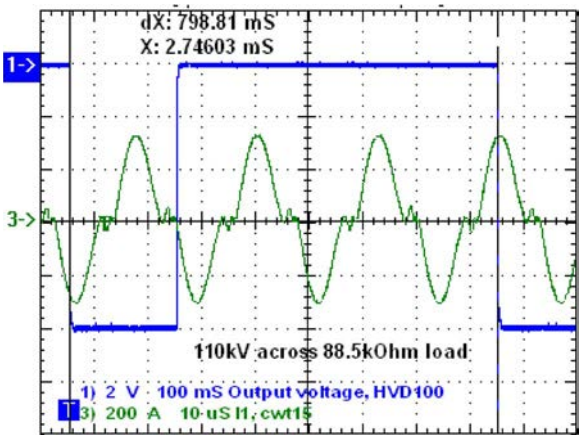


Fig. 13. Long-pulse operation: 110 kV, 137-kW peak power, and 34-kW average power. (Trace 1) Load voltage and (trace 3) primary current (after voltage settling) are shown on different timescales. Nominal line.

0.8 s and a pulsewidth of 0.2 s across an 88.5-kΩ load, which corresponds to 137-kW peak power and 34-kW average power, respectively (see Fig. 13). At the time of writing this paper, a total of $1.1 \cdot 10^6$ pulses have been generated.

Additional pulse tests were made with a capacitive load imitating large ESP fields. With this purpose, a 0.4-$\mu$F capacitor was connected across a 180-kΩ load. The experiments were conducted at a repetition rate of ~0.2 Hz. The rise time from zero to 100 kV was 20 ms.

The unit was also tested for spark/arc withstand capability. It was repetitively shorted to ground at full voltage. No damage was sustained, also after intermittent sparking in the course of the tests. We note that the arc/spark protection is provided by a proprietary $L-R$ network limiting the current derivative and amplitude without significant power dissipation in this network (less than 10 W) in normal operation.

## V. CONCLUSION

An HVPS for long-pulse applications has been developed. It was extensively tested in a wide range of resistive and capacitive loads. The HVPS salient features are as follows:

1) multiphase topology and modular construction allow easy and fast tailoring of HVPS for specific needs;
2) exceptionally low ripple and fast rise time combined with low stored energy;
3) high efficiency and PF in a wide range of output parameters;
4) all-air-cooled design;
5) small size, weight, and footprint; small oil volume.

It is foreseen that the described approach will be widely implemented in HVPS for long-pulse applications, particularly for X-ray computer tomography scanners.

## ACKNOWLEDGMENT

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